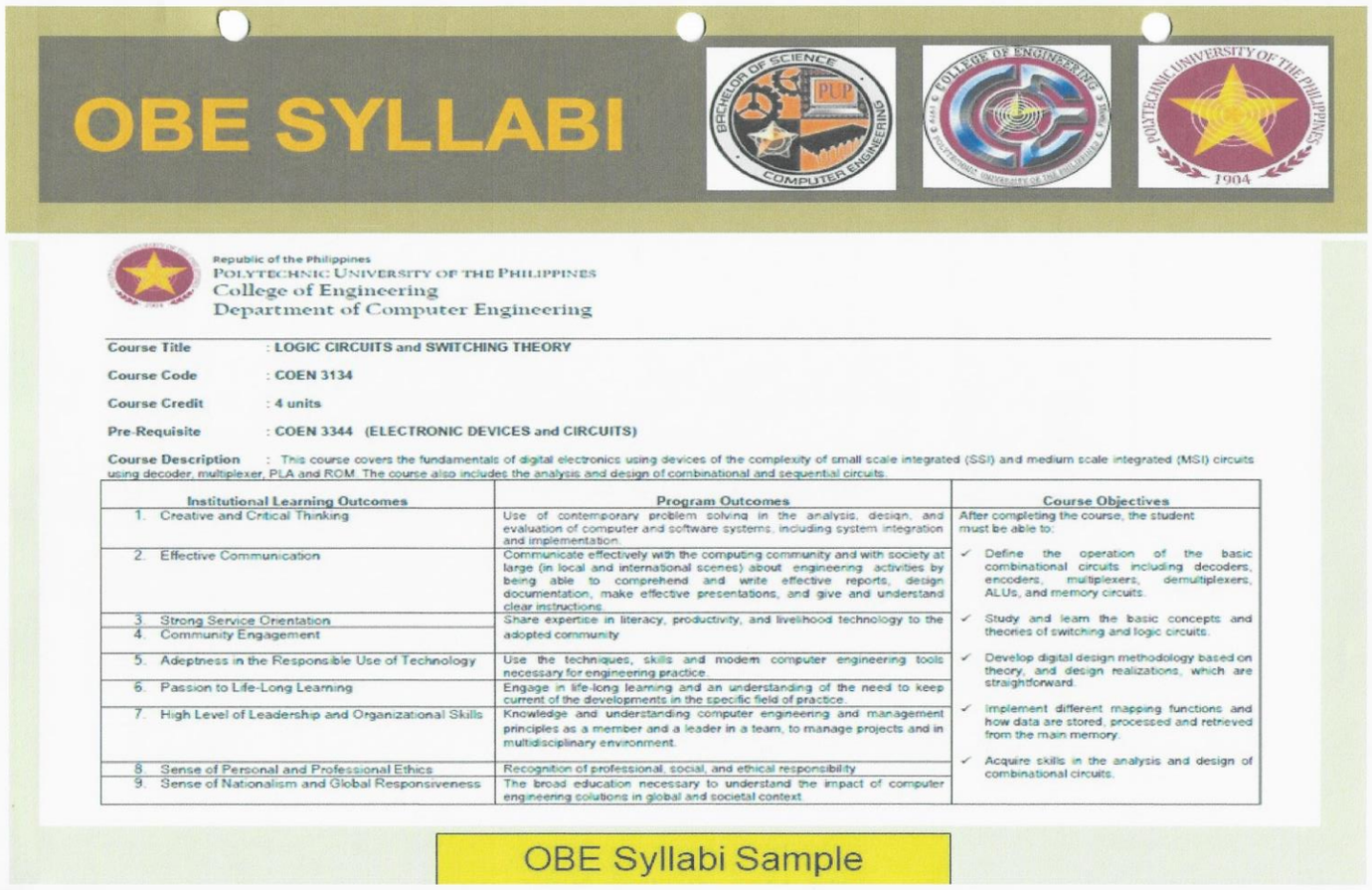
OBE SYLLABI



Republic of the Philippines
POLYTECHNIC UNIVERSITY OF THE PHILIPPINES
College of Engineering
Department of Computer Engineering

Course Title : **LOGIC CIRCUITS and SWITCHING THEORY**

Course Code : **COEN 3134**

Course Credit : **4 units**

Pre-Requisite : **COEN 3344 (ELECTRONIC DEVICES and CIRCUITS)**

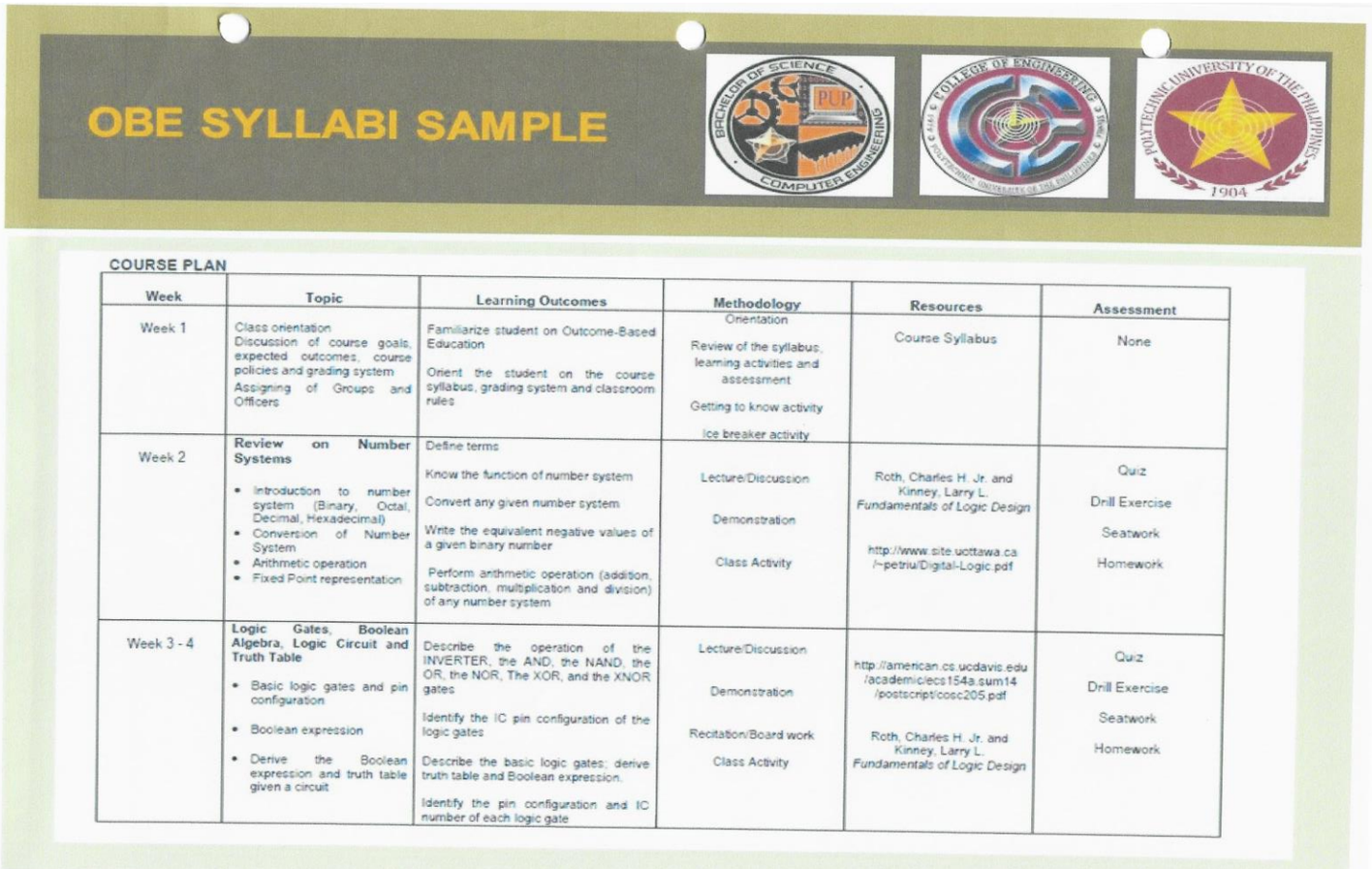
Course Description : This course covers the fundamentals of digital electronics using devices of the complexity of small scale integrated (SSI) and medium scale integrated (MSI) circuits using decoder, multiplexer, PLA and ROM. The course also includes the analysis and design of combinational and sequential circuits.

Institutional Learning Outcomes	Program Outcomes	Course Objectives
1. Creative and Critical Thinking	Use of contemporary problem solving in the analysis, design, and evaluation of computer and software systems, including system integration and implementation.	After completing the course, the student must be able to: ✓ Define the operation of the basic combinational circuits including decoders, encoders, multiplexers, demultiplexers, ALUs, and memory circuits. ✓ Study and learn the basic concepts and theories of switching and logic circuits. ✓ Develop digital design methodology based on theory, and design realizations, which are straightforward. ✓ Implement different mapping functions and how data are stored, processed and retrieved from the main memory. ✓ Acquire skills in the analysis and design of combinational circuits.
2. Effective Communication	Communicate effectively with the computing community and with society at large (in local and international scenes) about engineering activities by being able to comprehend and write effective reports, design documentation, make effective presentations, and give and understand clear instructions.	
3. Strong Service Orientation 4. Community Engagement	Share expertise in literacy, productivity, and livelihood technology to the adopted community	
5. Adeptness in the Responsible Use of Technology	Use the techniques, skills and modern computer engineering tools necessary for engineering practice.	
6. Passion to Life-Long Learning	Engage in life-long learning and an understanding of the need to keep current of the developments in the specific field of practice.	
7. High Level of Leadership and Organizational Skills	Knowledge and understanding computer engineering and management principles as a member and a leader in a team, to manage projects and in multidisciplinary environment.	
8. Sense of Personal and Professional Ethics	Recognition of professional, social, and ethical responsibility	
9. Sense of Nationalism and Global Responsiveness	The broad education necessary to understand the impact of computer engineering solutions in global and societal context.	

OBE Syllabi Sample

(02) 8713 5968 | dcoe_chair@gmail.com
RM322 CEA BLDG. NDC COMPOUND,
ANONAS COR. PUREZA STREETS, STA. MESA, MANILA

OBE SYLLABI SAMPLE



COURSE PLAN

Week	Topic	Learning Outcomes	Methodology	Resources	Assessment
Week 1	Class orientation Discussion of course goals, expected outcomes, course policies and grading system Assigning of Groups and Officers	Familiarize student on Outcome-Based Education Orient the student on the course syllabus, grading system and classroom rules	Orientation Review of the syllabus, learning activities and assessment Getting to know activity Ice breaker activity	Course Syllabus	None
Week 2	**Review on Number Systems** • Introduction to number system (Binary, Octal, Decimal, Hexadecimal) • Conversion of Number System • Arithmetic operation • Fixed Point representation	Define terms Know the function of number system Convert any given number system Write the equivalent negative values of a given binary number Perform arithmetic operation (addition, subtraction, multiplication and division) of any number system	Lecture/Discussion Demonstration Class Activity	Roth, Charles H. Jr. and Kinney, Larry L. *Fundamentals of Logic Design* http://www.site.uottawa.ca/~petriu/Digital-Logic.pdf	Quiz Drill Exercise Seatwork Homework
Week 3 - 4	**Logic Gates, Boolean Algebra, Logic Circuit and Truth Table** • Basic logic gates and pin configuration • Boolean expression • Derive the Boolean expression and truth table given a circuit	Describe the operation of the INVERTER, the AND, the NAND, the OR, the NOR, The XOR, and the XNOR gates Identify the IC pin configuration of the logic gates Describe the basic logic gates; derive truth table and Boolean expression. Identify the pin configuration and IC number of each logic gate	Lecture/Discussion Demonstration Recitation/Board work Class Activity	http://american.cs.ucdavis.edu/academic/ecs154a.sum14/postscript/cosc205.pdf Roth, Charles H. Jr. and Kinney, Larry L. *Fundamentals of Logic Design*	Quiz Drill Exercise Seatwork Homework

(02) 8713 5968 | dcoe_chair@gmail.com
RM322 CEA BLDG. NDC COMPOUND,
ANONAS COR. PUREZA STREETS, STA. MESA, MANILA

OBE SYLLABI SAMPLE

	• Derive the truth table and design the circuit given an expression • Derive the standard SOP and POS expression	Derive the Boolean expression and truth table given a logic circuit. Derive the truth table and design the circuit given a Boolean expression.			
Week 5	**Boolean Expression Simplification** • Discuss the Boolean identities • Application of De Morgan's Theorem • Simplifying an expression	Discuss the objectives of simplifying Boolean expressions Enumerate the methods of Boolean expressions simplification Acquaint themselves with Boolean Identities Apply De Morgan's Theorem to Boolean Expressions and to logic circuits	Lecture/Discussion Demonstration Recitation/Board work Class Activity	http://american.cs.ucdavis.edu/academic/ecs154a.sum14/postscript/cosc205.pdf Roth, Charles H. Jr. and Kinney, Larry L. *Fundamentals of Logic Design*	Quiz Drill Exercise Seatwork Homework
Week 6	**Conversion of any Product Term to Standard form and Conversion of any Sum Term to Standard form** • Discuss the procedure on how to convert an expression to its standard form	Determine the domain of a Boolean expression Convert any SOP expression to standard SOP Express SOP expression into Canonical Form Convert any POS expression to standard POS Express POS expression into Canonical Form	Lecture/Discussion Demonstration Recitation/Board work Class Activity	http://american.cs.ucdavis.edu/academic/ecs154a.sum14/postscript/cosc205.pdf Roth, Charles H. Jr. and Kinney, Larry L. *Fundamentals of Logic Design*	Quiz Drill Exercise Seatwork Homework

(02) 8713 5968 | dcoe_chair@gmail.com
RM322 CEA BLDG. NDC COMPOUND,
ANONAS COR. PUREZA STREETS, STA. MESA, MANILA

OBE SYLLABI SAMPLE

Week 7 - 8	**Karnaugh-map Simplification(SOP, POS and with don't care conditions)** • Discuss how to construct and fill out a K-map given a truth table, an expression or a notation • Discuss the steps in simplifying an expression using k-map • Discuss the rules in grouping of 1's/0's with don't care condition in k-map • Discuss how to derive the simplified expression using k-map	Differentiate Map method from Algebraic simplification technique Construct two-, three-, four-, and five-variable K-Maps Fill-out the K-map with terms from Sum-of-Products (SOP) expressions / Product-of-Sum (POS) Combine the 1s/0's on the map into largest group possible and into minimum number of groups Determine the product term/sum term for each group in the map Combine the minimum product terms/sum terms to form the simplified SOP/POS expressions Construct the circuit of the simplified SOP/POS expression (AND-OR Network/OR-AND Network) Describe don't care condition Simplify expressions with don't-care conditions	Lecture/Discussion Demonstration Recitation/Board work Class Activity	http://american.cs.ucdavis.edu/academic/ecs154a.sum14/postscript/cosc205.pdf Roth, Charles H. Jr. and Kinney, Larry L. *Fundamentals of Logic Design*	Quiz Drill Exercise Seatwork Homework

(02) 8713 5968 | dcoe_chair@gmail.com
RM322 CEA BLDG. NDC COMPOUND,
ANONAS COR. PUREZA STREETS, STA. MESA, MANILA

OBE SYLLABI SAMPLE

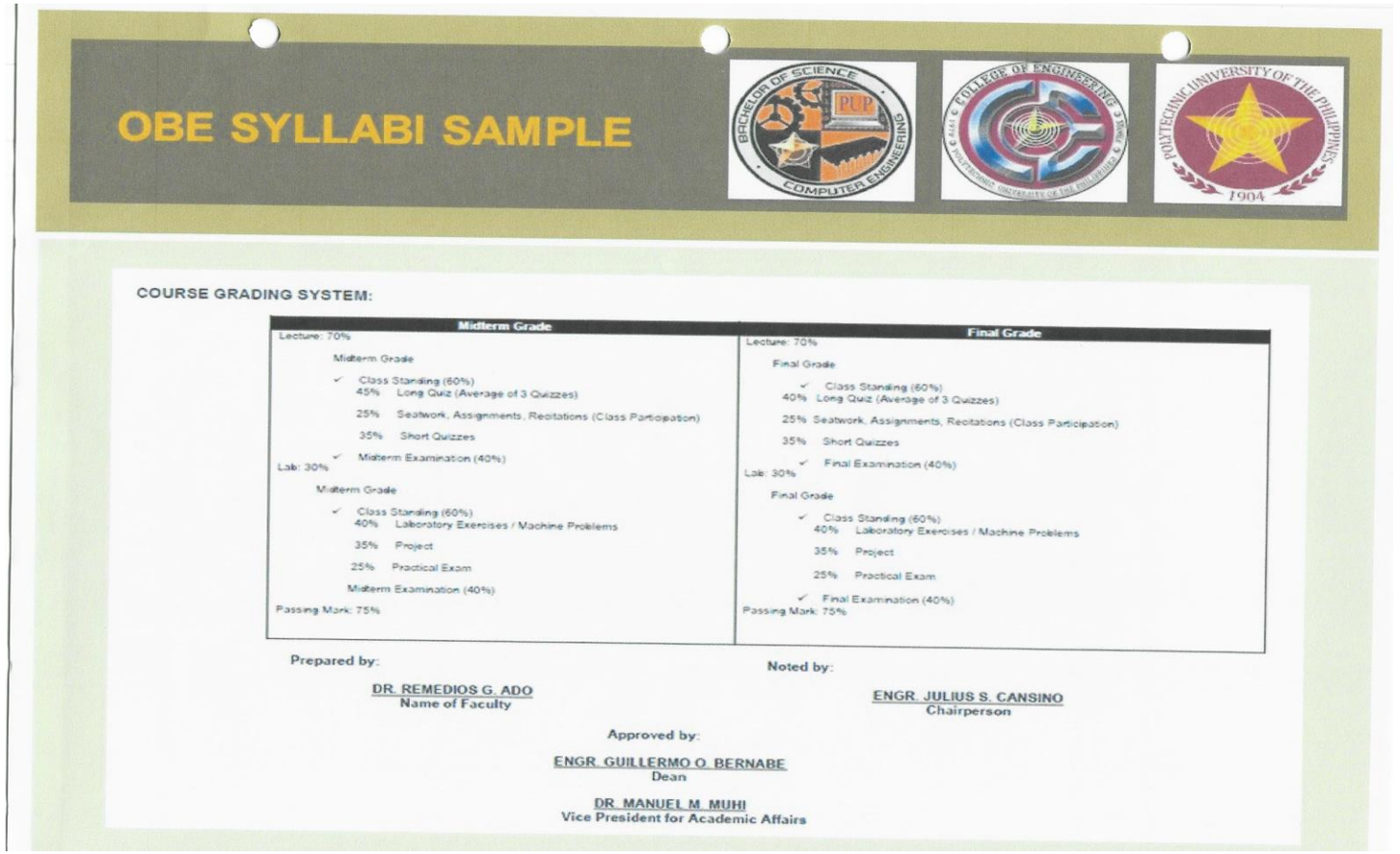
Week 9	**MIDTERM EXAM**				
Week 10 – 11	**Other Two-level Implementations (SOP/POS)** • Discuss how to derive and construct a combinational circuit using other SOP Networks • Discuss how to derive and construct circuit using other SOP Networks • Discuss the steps ton how to design a combinational circuit • Discuss how to determine the number of input and output variables need based on the given problems statement	Construct the logic circuit of the simplified SOP expression using the NAND – NAND, OR – NAND & NOR – OR network Construct the logic circuit of the simplified POS expressions using the NOR – NOR, AND – NOR, NAND – AND network Describe the operation of a Decoder Implement Boolean function using a Decoder	Lecture/Discussion Demonstration Recitation/ Board work Class Activity	http://american.cs.ucdavis.edu/academic/ecs154a.sum14/postscript/cosc205.pdf Roth, Charles H. Jr. and Kinney, Larry L. *Fundamentals of Logic Design*	Quiz Drill Exercise Seatwork Homework
Week 12 - 13	**Combinational Circuit Design using MSI and LSI Devices (Decoder)** • Discuss how to design a combinational circuit using MSI Device (Decoder) given a problem statement • Discuss how to design a combinational circuit using MSI Device (Multiplexer) given a notation	Describe the operation of a Multiplexer implement Boolean function using a Multiplexer	Lecture/Discussion Demonstration Recitation/Board work Class Activity	http://american.cs.ucdavis.edu/academic/ecs154a.sum14/postscript/cosc205.pdf Roth, Charles H. Jr. and Kinney, Larry L. *Fundamentals of Logic Design*	Quiz Drill Exercise Seatwork Homework

(02) 8713 5968 | dcoe_chair@gmail.com
RM322 CEA BLDG. NDC COMPOUND,
ANONAS COR. PUREZA STREETS, STA. MESA, MANILA

OBE SYLLABI SAMPLE

Week 14 - 15	**Combinational Circuit Design using MSI and LSI Devices** • Discuss how to design a combinational circuit using MSI Device (ROM) given a notation • Discuss how to design a combinational circuit using MSI Device (PLA) given a notation	Describe the operation of a Read-Only Memory (ROM) Implement Boolean function using a ROM Describe the operation of a Programmable Logic Array (PLA) Implement Boolean functions using PLA	Lecture/Discussion Demonstration Recitation/Board work Class Activity	http://american.cs.ucdavis.edu/academic/ecs154a.sum14/postscript/cosc205.pdf Roth, Charles H. Jr. and Kinney, Larry L. *Fundamentals of Logic Design*	Quiz Drill Exercise Seatwork Homework Practical Exam
Week 16	**APPLICATION PROJECT PRESENTATION**	Culminating activity given to the grouped students to test their mastery of the course by developing application design utilizing all the theories and concepts acquired	Project Presentation System Walk-through Prototype Demonstration	*Application Project Documentation* *Developed System*	Project Deliberation
Week 17	**APPLICATION PROJECT PRESENTATION**	Culminating activity given to the students to test their mastery of the course by developing application design utilizing all the theories and concepts acquired	Project Presentation System Walk-through Prototype Demonstration	*Application Project Documentation* *Developed System*	Project Deliberation
Week 18	**FINAL EXAMINATION**				

(02) 8713 5968 | dcoe_chair@gmail.com
RM322 CEA BLDG. NDC COMPOUND,
ANONAS COR. PUREZA STREETS, STA. MESA, MANILA



OBE SYLLABI SAMPLE

COURSE GRADING SYSTEM:

Midterm Grade	Final Grade
Lecture: 70% Midterm Grade ✓ Class Standing (60%) 45% Long Quiz (Average of 3 Quizzes) 25% Seatwork, Assignments, Recitations (Class Participation) 35% Short Quizzes ✓ Midterm Examination (40%) Lab: 30% Midterm Grade ✓ Class Standing (60%) 40% Laboratory Exercises / Machine Problems 35% Project 25% Practical Exam Midterm Examination (40%) Passing Mark: 75%	Lecture: 70% Final Grade ✓ Class Standing (60%) 40% Long Quiz (Average of 3 Quizzes) 25% Seatwork, Assignments, Recitations (Class Participation) 35% Short Quizzes ✓ Final Examination (40%) Lab: 30% Final Grade ✓ Class Standing (60%) 40% Laboratory Exercises / Machine Problems 35% Project 25% Practical Exam ✓ Final Examination (40%) Passing Mark: 75%

Prepared by:

DR. REMEDIOS G. ADO
Name of Faculty

Noted by:

ENGR. JULIUS S. CANSINO
Chairperson

Approved by:

ENGR. GUILLERMO O. BERNABE
Dean

DR. MANUEL M. MUHI
Vice President for Academic Affairs

(02) 8713 5968 | dcoe_chair@gmail.com
RM322 CEA BLDG. NDC COMPOUND,
ANONAS COR. PUREZA STREETS, STA. MESA, MANILA

POLYTECHNIC UNIVERSITY OF THE PHILIPPINES

College of Engineering

Computer Engineering Department

Tel No: 713-5968

School Year 2010-2011

COURSE CODE: COEN 3094

COURSE TITLE: Circuits2

COURSE CREDIT: 4 units

PRE-REQUISITE: Circuits 1

I. COURSE DESCRIPTION:

Complex algebra and phasors; simple AC circuits, impedance and admittance; mesh and node analysis for AC circuits; AC network theorems; power in AC circuits; resonance; three-phase circuits; transformers; two-port network parameters and transfer function.

II. COURSE CONTENT (OUTLINE):

1. Complex Algebra and Phasors
2. Impedance and Admittance
1. Simple AC Circuits
2. Transformers
3. Resonance
4. Mesh and Node Analysis for AC Circuits
5. AC Network Theorems
6. Power in AC Circuits
7. Three-Phase Circuits
8. Two-Port Network Parameters and Transfer Function

III. STRATEGIES AND METHODS OF TEACHING:

1. Lecture/Discussion
2. Assignment

IV. REQUIREMENTS

- Quizzes
- Examinations
- Class Participations (i.e. Assignment, Seatwork, Recitation, Attendance)

V. GRADING SYSTEM:

Midterm = [(Q1+Q2+Q3)/3] 30% + CS 20% + (Midterm Exam) 50%
Final = [(Q1+Q2+Q3)/3] 30% + CS 20% + (Final Exam) 50%
General Average = (Midterm) 50% + (Final) 50%

POLYTECHNIC UNIVERSITY OF THE PHILIPPINES

College of Engineering

Computer Engineering Department

Tel No: 713-5968

School Year 2010-2011

COURSE CODE: COEN 3174

COURSE TITLE: Advanced Logic Circuit

COURSE CREDIT: 4 units

PRE-REQUISITE: Logic Circuits Switching Theory

I. COURSE DESCRIPTION:

This course on digital design focuses on different methodologies and styles in hardware modeling with emphasis on the use of hardware description languages (HDLs). It covers very high speed integrated circuit hardware description language (VHDL) fundamental language concepts and elements and the different levels of descriptions such as behavioral and structural.

II. COURSE CONTENT (OUTLINE):

1. Introduction
2. Algorithm State Machines
   - 2.1 ASM Chart
   - 2.2 Control implementation
   - 2.3 Design with Multiplexes
3. Overview of Digital Systems
   - 3.1 Evolution of Digital System Design Methodology
   - 3.2 Different Hardware Description Languages (HDLs)
   - 3.3 History of VHDL
   - 3.4 Advantages and Disadvantages of VHDL
4. VHDL-Related Technologies and Fields
   - 4.1 PLDs
5. Hardware Modeling using VHDL
   - 5.1 Levels of Modeling or Abstraction
   - 5.2 VHDL Model Components or Structural Elements
6. VHDL Language
   - 6.1 Lexical Elements
   - 6.2 Scalar Data Types
   - 6.3 Expressions and Operators
   - 6.4 Control Structures
7. VHDL Language
   - 7.1 Composite Data Types
   - 7.2 Access Types
   - 7.3 File Types
8. Basic Modeling Concepts
9. Subprogram and Packages
10. Algorithmic State Machines
    - 10.1 ASM Charts
    - 10.2 Control Implementation
    - Design with Multiplexers

III. STRATEGIES AND METHODS OF TEACHING:

1. Lecture/Discussion
2. Assignment

IV. REQUIREMENTS

- Quizzes
- Examinations
- Class Participations (i.e. Assignment, Seatwork, Recitation, Attendance)

V. REFERENCE:

- Peter Ashenden. The Designer's Guide to VHDL Francisco, CA 2nd edition
- James Armstrong and F. Gail Gray. VHDL Representation and Synthesis. 2nd edition.
- Ulrish Heinkel. The VHDL Reference: A Practical Guide Computer Aided Integrated Circuit Design Includes V AMS
- Douglas Perry. VHDL. 3rd edition.
- IEEE Standard VHDL Language Reference Manual Std 1076-1993-USA
- Ben Cohen. VHDL Coding Styles and Methodologists Ed.
- Zainalabedin Navabi. VHDL: Analysis and Modelling Digital Systems. 2nd edition.
- Kevin Shakill. VHDL for Programmable Logic.

VI. GRADING SYSTEM:

Midterm = [(Q1+Q2+Q3)/3] 30% + CS 20% + (Midterm Exam) 50%
Final = [(Q1+Q2+Q3)/3] 30% + CS 20% + (Final Exam) 50%
General Average = (Midterm) 50% + (Final) 50%

Signed by:

ENGR. REMEDIOS G. ADO
Chairperson, CoE Department

DR. MANUEL M. MUHI
Dean, CE

POLYTECHNIC UNIVERSITY OF THE PHILIPPINES

College of Engineering

Computer Engineering Department

Tel No: 713-5968

School Year 2010-2011

COURSE CODE: COEN 3064

COURSE TITLE: Circuits1

COURSE CREDIT: 4 units

PRE-REQUISITE: Physics 2, Integral Calculus

I. COURSE DESCRIPTION:

Fundamental relationships in circuit theory, mesh and node equations; resistive networks, network theorems; solutions of network problems using Laplace transform; transient analysis; methods of circuit analysis.

II. COURSE CONTENT (OUTLINE):

1. Fundamental Relationship in Circuit Theory
2. Resistive Network
3. Mesh and Node Equations
4. Network Theorems
5. Transient Analysis
6. Solution of Network Problems Using Laplace Transform
   Methods of Analysis for Special Circuits

III. STRATEGIES AND METHODS OF TEACHING:

1. Lecture/Discussion
2. Assignment

IV. REQUIREMENTS

- Quizzes
- Examinations
- Class Participations (i.e. Assignment, Seatwork, Recitation, Attendance)

V. GRADING SYSTEM:

Midterm = [(Q1+Q2+Q3)/3] 30% + CS 20% + (Midterm Exam) 50%
Final = [(Q1+Q2+Q3)/3] 30% + CS 20% + (Final Exam) 50%
General Average = (Midterm) 50% + (Final) 50%

Signed by:

ENGR. REMEDIOS G. ADO
Chairperson, CoE Department

DR. MANUEL M. MUHI
Dean, CE

(02) 8713 5968 | dcoe_chair@gmail.com
RM322 CEA BLDG. NDC COMPOUND,
ANONAS COR. PUREZA STREETS, STA. MESA, MANILA

POLYTECHNIC UNIVERSITY OF THE PHILIPPINES

College of Engineering

Computer Engineering Department

Tel No: 713-5968

School Year 2010-2011

COURSE CODE: COEN 3094

COURSE TITLE: Circuits2

COURSE CREDIT: 4 units

PRE-REQUISITE: Circuits 1

I. COURSE DESCRIPTION:

Complex algebra and phasors; simple AC circuits, impedance and admittance; mesh and node analysis for AC circuits; AC network theorems; power in AC circuits; resonance; three-phase circuits; transformers; two-port network parameters and transfer function.

II. COURSE CONTENT (OUTLINE):

1. Complex Algebra and Phasors
2. Impedance and Admittance
1. Simple AC Circuits
2. Transformers
3. Resonance
4. Mesh and Node Analysis for AC Circuits
5. AC Network Theorems
6. Power in AC Circuits
7. Three-Phase Circuits
8. Two-Port Network Parameters and Transfer Function

III. STRATEGIES AND METHODS OF TEACHING:

1. Lecture/Discussion
2. Assignment

IV. REQUIREMENTS

- Quizzes
- Examinations
- Class Participations (i.e. Assignment, Seatwork, Recitation, Attendance)

V. GRADING SYSTEM:

Midterm = [(Q1+Q2+Q3)/3] 30% + CS 20% + (Midterm Exam) 50%
Final = [(Q1+Q2+Q3)/3] 30% + CS 20% + (Final Exam) 50%
General Average = (Midterm) 50% + (Final) 50%

POLYTECHNIC UNIVERSITY OF THE PHILIPPINES

College of Engineering

Computer Engineering Department

Tel No: 713-5968

School Year 2010-2011

COURSE CODE: COEN 3174

COURSE TITLE: Advanced Logic Circuit

COURSE CREDIT: 4 units

PRE-REQUISITE: Logic Circuits Switching Theory

I. COURSE DESCRIPTION:

This course on digital design focuses on different methodologies and styles in hardware modeling with emphasis on the use of hardware description languages (HDLs). It covers very high speed integrated circuit hardware description language (VHDL) fundamental language concepts and elements and the different levels of descriptions such as behavioral and structural.

II. COURSE CONTENT (OUTLINE):

1. Introduction
2. Algorithm State Machines
   - 2.1 ASM Chart
   - 2.2 Control implementation
   - 2.3 Design with Multiplexes
3. Overview of Digital Systems
   - 3.1 Evolution of Digital System Design Methodology
   - 3.2 Different Hardware Description Languages (HDLs)
   - 3.3 History of VHDL
   - 3.4 Advantages and Disadvantages of VHDL
4. VHDL-Related Technologies and Fields
   - 4.1 PLDs
5. Hardware Modeling using VHDL
   - 5.1 Levels of Modeling or Abstraction
   - 5.2 VHDL Model Components or Structural Elements
6. VHDL Language
   - 6.1 Lexical Elements
   - 6.2 Scalar Data Types
   - 6.3 Expressions and Operators
   - 6.4 Control Structures
7. VHDL Language
   - 7.1 Composite Data Types
   - 7.2 Access Types
   - 7.3 File Types
8. Basic Modeling Concepts
9. Subprogram and Packages
10. Algorithmic State Machines
    - 10.1 ASM Charts
    - 10.2 Control Implementation
    - Design with Multiplexers

III. STRATEGIES AND METHODS OF TEACHING:

1. Lecture/Discussion
2. Assignment

IV. REQUIREMENTS

- Quizzes
- Examinations
- Class Participations (i.e. Assignment, Seatwork, Recitation, Attendance)

V. REFERENCE:

- Peter Ashenden. The Designer's Guide to VHDL Francisco, CA 2nd edition
- James Armstrong and F. Gail Gray. VHDL Representation and Synthesis. 2nd edition.
- Ulrish Heinkel. The VHDL Reference: A Practical Guide Computer Aided Integrated Circuit Design Includes V AMS
- Douglas Perry. VHDL. 3rd edition.
- IEEE Standard VHDL Language Reference Manual Std 1076-1993-USA
- Ben Cohen. VHDL Coding Styles and Methodologists Ed.
- Zainalabedin Navabi. VHDL: Analysis and Modelling Digital Systems. 2nd edition.
- Kevin Shakill. VHDL for Programmable Logic.

VI. GRADING SYSTEM:

Midterm = [(Q1+Q2+Q3)/3] 30% + CS 20% + (Midterm Exam) 50%
Final = [(Q1+Q2+Q3)/3] 30% + CS 20% + (Final Exam) 50%
General Average = (Midterm) 50% + (Final) 50%

Signed by:

ENGR. REMEDIOS G. ADO
Chairperson, CoE Department

DR. MANUEL M. MUHI
Dean, CE

POLYTECHNIC UNIVERSITY OF THE PHILIPPINES

College of Engineering

Computer Engineering Department

Tel No: 713-5968

School Year 2010-2011

COURSE CODE: COEN 3064

COURSE TITLE: Circuits1

COURSE CREDIT: 4 units

PRE-REQUISITE: Physics 2, Integral Calculus

I. COURSE DESCRIPTION:

Fundamental relationships in circuit theory, mesh and node equations; resistive networks, network theorems; solutions of network problems using Laplace transform; transient analysis; methods of circuit analysis.

II. COURSE CONTENT (OUTLINE):

1. Fundamental Relationship in Circuit Theory
2. Resistive Network
3. Mesh and Node Equations
4. Network Theorems
5. Transient Analysis
6. Solution of Network Problems Using Laplace Transform
   Methods of Analysis for Special Circuits

III. STRATEGIES AND METHODS OF TEACHING:

1. Lecture/Discussion
2. Assignment

IV. REQUIREMENTS

- Quizzes
- Examinations
- Class Participations (i.e. Assignment, Seatwork, Recitation, Attendance)

V. GRADING SYSTEM:

Midterm = [(Q1+Q2+Q3)/3] 30% + CS 20% + (Midterm Exam) 50%
Final = [(Q1+Q2+Q3)/3] 30% + CS 20% + (Final Exam) 50%
General Average = (Midterm) 50% + (Final) 50%

Signed by:

ENGR. REMEDIOS G. ADO
Chairperson, CoE Department

DR. MANUEL M. MUHI
Dean, CE

(02) 8713 5968 | dcoe_chair@gmail.com
RM322 CEA BLDG. NDC COMPOUND,
ANONAS COR. PUREZA STREETS, STA. MESA, MANILA

COPIES OF ALL COURSE SYLLABI

(See Separate Exhibit)

(02) 8713 5968 | dcoe_chair@gmail.com
RM322 CEA BLDG. NDC COMPOUND,
ANONAS COR. PUREZA STREETS, STA. MESA, MANILA